Metal-oxide semiconductor field-effect transistor

_A lab exercise in the course FFFF10/FYSD13: Processing and Device Technology_

**Introduction**

During this lab exercise you and your lab partners will process silicon-on-insulator MOSFETs using techniques that are similar to those used in semiconductor laboratories. This is an extensive lab exercise which consists of four half days of lab work.

**Background**

Since the breakthrough of modern electronics in the mid 1950’s the most important electronic device has been the transistor. The transistor is a so-called three terminal device, with three connectors to it. The basic principle of the transistor is that one can control a current flowing between two terminals, often called the _source_ and _drain_ contacts, by applying a voltage to the third terminal called the _gate_ contact. The most successful transistors to date are based on semiconductors, more specifically silicon (Si). These transistors can be found for example in your laptop, alarm clock and cell phone. Since the birth of the transistor, performance has been improved mainly by downscaling, thus also allowing more and more devices to be integrated onto the same chip area.

Although electronics have improved tremendously since the 1950’s, it is obvious that downscaling cannot continue indefinitely due to the finite size of the atom. Today, state-of-the-art transistors have oxide layers only a few atoms thick and gate terminals some tens of nanometers long. Different approaches will eventually be necessary to continue the improvement of electronic devices.

**SOI MOSFET**

In a silicon-on-insulator (SOI) transistor the transistor channel (Si) is situated on top of an insulating SiO₂ film rather than on Si with opposite doping type. The SOI technology offers lower leakage currents, reduced capacitance and improved low voltage operation. However, this comes at the expense of higher cost, and issues with heat dissipation and device variability.

Figure 1 shows a schematic image of the SOI MOSFET device structure processed in the lab exercises. This structure is strongly simplified compared to commercial transistors, such that it is possible for us to fabricate and characterize it in our four lab sessions. The starting material (wafer) for the lab exercises is comprised of a thick bottom slab of Si (675 µm), an intermediate insulating SiO₂ film (0.5 µm) followed by a Si top film (~1 µm thick, p-doped 10¹⁶ cm⁻³). This top-most Si film will be referred to as the _channel_. On top of the channel three contacts will be processed, constituting the _source_, _gate_ and _drain_ electrodes. Beneath the _gate_ will be an ultra-thin insulating film (either SiO₂ or SiO₂/HfO₂) that prevents current from flowing from the _gate_ into the _channel_.

![Figure 1. Schematic image of the SOI MOSFET showing the contacts on top, the gate oxide, the channel, the lower insulator, and finally the substrate.](image)
Principles of operation

Here follows a brief explanation of the operation of the type of $p$-channel MOSFET that we are studying in the lab exercise. Please note that the structure we are fabricating is not a conventional MOSFET, but a hybrid between a MOSFET and a MESFET (metal-semiconductor field-effect transistor, see p. 240 in the course book). Our device will only have one doping type ($p$, holes), and will be “normally on” (depletion-mode). Conventional MOSFETs used in digital applications have both $p$- and $n$-doped regions, and are “normally off” (enhancement mode), which is important for lowering the power consumption.

In the figure below the operation principles for a $p$-MOSFET is described (operated opposite to the $n$-MOSFET on p. 240): Assume that we keep the source grounded and that a negative voltage is applied to the drain ($V_D < 0$), so that holes flow from source to drain. At small negative drain voltages, the drain current will increase linearly with applied drain voltage according to Ohm’s law (Figure 2a).

However, as $V_D$ continues to become more negative, the hole concentration in the part of the channel near the gate-drain junction will be reduced. At some point “pinch-off” is reached, where the Si channel region near the drain is depleted of holes all the way down to the SiO$_2$ film. A region of higher resistance now develops under the gate, which expands with more negative $V_D$ towards the source, in a way that the channel resistance ($R_{\text{channel}}$) is roughly proportional to $V_D$, and therefore $I_D = V_D/R_{\text{channel}} \sim \text{constant}$. The maximum current through the transistor is called the saturation current (Figure 2b and 2c).

The level of saturation current can be controlled by the applied gate voltage. For example, when a positive voltage is applied to the gate, parts of the channel will be depleted even without an applied source-drain voltage, and pinch-off is reached earlier. The saturation current will then be lower (Figure 2d). A very high positive gate voltage will deplete the channel of holes already at zero drain voltage and no current at all can flow through the channel. The transistor will then be turned off completely. Note however that external factors, such as incoming light or elevated temperatures, can generate charge carriers and deteriorate the transistor properties.
Figure 2. Variation of depletion layer width and output characteristics of a p-channel MOSFET (oxide is not shown) under various biasing conditions (note: $V_D$ is negative). Image adapted from Sze and Lee 2012, p. 242.
Methods

The lab exercise is divided into four sessions each starting with a briefing from the lab supervisors. The lab work will be conducted inside a clean room. Here follows some important rules which must be followed during the lab exercise:

- Be careful, and do not rush!

The cleanroom process contains many steps which are all important for how the end result will turn out. It is crucial to always take extra care with your work, as it is not possible to start over.

- Always follow the instructions precisely!

The safety of both you, those around you, and the equipment used relies on that you work in a safe way. You therefore need to follow the instructions of the lab supervisor. Also, the end result of the transistor depends on how well you followed the instructions.

Transistor design

The MOSFETs that will be processed in this series of lab exercises have a circular geometry, with a circular source contact in the center surrounded by two concentric rings functioning as gate and drain contact. Many devices will be processed simultaneously on one sample, with varying gate lengths and distance between source and drain. By using the circular geometry we remove the need for isolating the devices from each other by a so-called mesa-etch. A scanning electron microscope image of a transistor and a cross section of the transistor beneath the gate contact are shown in Figure 3.

![Figure 3. The MOSFET design. (a) Several circular devices at 80° tilt angle. The center circle is the source contact, the middle ring is the gate contact and the outer ring is the drain contact. (b) Three tungsten probes brought into contact with the source, gate and drain contact for electrical characterization.](image-url)
Purpose and general outline of the four lab sessions

Here follows a brief description of what the different parts of the lab will contain. The details will be provided during the lab exercise. As homework after Session 2, you will propose a list of process steps to be used in Session 3.

Session 1 – Defining the Source and Drain contacts
Preparation: Read about optical lithography, Sze p.428-441
- Longer briefing
- Prepare samples with photosensitive resist (real samples and test samples for Session 3)
- Photolithography using mask for Source and Drain contacts.

Homework: Write a preliminary report about the activities in Session 1

Session 2 – Annealing and oxide deposition
- Shorter briefing
- Lift-off
- Contact anneal
- Deposit gate oxide using Atomic Layer Deposition (on samples with thin SiO₂)
- Side activity: Metal sputtering on organic samples for Session 4.

Homework: Write a preliminary report about the activities in Session 2. Design a suggested process flow, including all individual process steps, for Session 3.

Session 3 – Defining the Gate contact
Preparation: Read about dry etching: p.450-453
- Quick briefing
- Ellipsometry of the HfO₂ film grown in Session 2
- Photolithography using mask for Gate contact.
- Dry etching using oxygen plasma

Homework: Write a preliminary report about the activities in Session 3.

Session 4 – Measurements
Preparation: Reread the section about the MOSFET in this manual.
- Quick briefing
- Electrical measurements on your transistors using a probe station.
- Characterization of your transistors and biological samples using a scanning electron microscope.

Homework: Write a complete lab report (see below) based on your earlier (personal) reports and email it as a pdf to the course responsible (Claes Thelander).
Lab report

Lab reports are written individually. The deadline for submitting your lab report is 1 week after your last lab (Lab 4). However, it is necessary that you start writing your report directly after Lab 1. Otherwise you may risk forgetting important information, and also have less time to prepare for the exam.

Plagiarism is not allowed! This includes copying text and/or figures from other lab reports, books or internet sources. If you are uncertain of what is considered plagiarism, please contact your lab supervisor.

Listed below are important guidelines for the structure of your lab report:

- The report is written individually and should cover all four lab sessions.
- The language is English.
- The length should be 1500-2500 words.
- The report should include:
  - An introduction, explaining the purpose of the lab exercise.
  - Thorough documentation of all process steps, explaining the purpose of the step, and short descriptions of the process techniques and equipment that were used. (Note: A detailed description of a particular process step carried out multiple times needs to be provided only once in the report)
  - Schematic illustrations (Hint: PowerPoint) of the device after key processing steps.
  - Optical images and SEM images (include scale bars where appropriate!)
  - Short description of transistor operation.
  - Results from the DC measurements (include figure legend where appropriate!).
  - A figure showing the output characteristics ($I_d$ vs $V_d$).
  - Two figures showing the transfer characteristics ($I_d$ vs $V_g$) and transcondutance $(dI/dV_g)$ vs $V_g$. Also explain how you obtained your $dI/dV_g$ values.
  - If $I_d$ could be modulated by at least two orders of magnitude: Provide a figure showing the so-called subthreshold slope ($\log(I_d)$ vs $V_g$). Extract the minimum $\Delta V_g$ required to change $I_d$ by one order of magnitude? (Hint: where is the slope steepest?)
  - Were the results from SEM and electrical measurements what you expected?
  - Discuss how the device performance can be improved.
  - How could the processing be improved to obtain a better yield?

- Reports must be handed in within 1 week after the final lab session.
- The report should be sent by email (in pdf-format) to claes.thelander@ftf.lth.se, please make sure the size of the file is well below 10 MB!!
- Previous years we have checked student reports for plagiarism by Urkund (http://www.urkund.se), and we intend to do so again this year.

Good Luck!